REMARKS

SUMMARY

Reconsideration of the application is respectfully requested.

Claims 1-3 and 15-25 remain in the application. Claims 1-3 and 15-25 are subject to examination and claims 4-14 were previously withdrawn from examination.

Applicants appreciatively acknowledge the Examiner's consideration and acceptance of the drawings filed on March 31, 2004.

RESPONSE TO EXAMINER'S RESPONSE TO ARGUMENTS

Applicants appreciatively acknowledge the Examiners consideration in "Response to Arguments," item 4 on page 3 of the Applicants' previous arguments. However, it appears from the Examiner's response that claims 1-3 and 15-25 are rejected based on facts within the personal knowledge of the Examiner. Thus, according to 37 C.F.R. § 1.104(d)(2), Applicant hereby requests an affidavit from the Examiner supporting the assertions on which this rejection is based.

More specifically, the Examiner indicates that when the "structures are planarized with the dielectric layer" the "difference between any two may be virtually 0nm" in item 4 on page 3 of the final Office Action and uses this information as a basis for rejection of the claims. As there is no indication that a difference of "virtually 0nm" has been achieved between the copper structures 233u in the '772 reference, Applicants respectfully request the affidavit from the Examiner supporting the assertions.

Applicants respectfully note that the semiconductor industry is continually trying to reduce the difference between such structures and that a difference of "virtually 0nm" would have been a notable achievement worthy of mention in the reference. Instead, Applicants submit that the '772 reference indicates in paragraph **[0019]** that "the conductors 233*u* extend above the upper interconnect layer to a height of between 10 and 500nm." Resulting in a

variability of 490 nm between conductor heights, not "5 nm or less" as recited in claims 1 and 15 or "in a range of 1nm to 5nm" as recited in claims 19 and 22.

With respect to the '650 reference, the Applicants acknowledge the Examiner's position that the inter-pillar spacing 290 of the '650 reference is at best 3-5 μm (300-500nm). However, the '650 reference also states that after bonding the intersubstrate spacing is "0.01- 0.2 μm" which constitutes a range of 10nm to 200nm or a disclosed resulting **variance of over 190nm**, not "5 nm or less" as recited in claims 1 and 15 or "in a range of 1nm to 5nm" as recited in claims 19 and 22.

SPECIFICATION AMENDMENTS

In the specification, Applicants have amended two previously overlooked typographical errors. The above-noted changes to the specification are provided solely for clarification or cosmetic reasons. The changes are neither provided to overcome the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

CLAIM REJECTIONS UNDER 35 U.S.C. § 102

In "Claim Rejections – 35 USC § 102," item 3 on page 2 of the above-identified final Office Action, claims 1-3 and 15-25 have been rejected as being fully anticipated by U.S. Published Patent Application No. US 2004/0262772 to *Ramanathan, et al.* (hereinafter "the '772 reference") or U.S. Published Patent Application No US 2005/0003650 to *Ramanathan, et al.* (hereinafter "the '650 reference") under 35 U.S.C. § 102(e). Applicants respectfully traverse.

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, an apparatus including:

> a first wafer having a first interlayer dielectric layer and a first plurality of copper structures of first substantially uniform heights with each difference between any two of the first substantially uniform heights being 5 nm or less, disposed on the first interlayer dielectric layer; and
>
> a second wafer having a second interlayer dielectric layer and a second plurality of copper structures of second substantially uniform heights with each difference between any two of the second substantially uniform heights being 5nm or less, disposed on the second interlayer dielectric layer, the second wafer being stacked on the first wafer, with at least some of the first and second plurality of copper structures being substantially aligned and bonded to each other.

Independent claim 15 includes similar language regarding "substantially uniform heights being 5 nm or less" as found in claim 1.

Independent claim 22 calls for, *inter alia*, a system including:

> a semiconductor package having
>
> a first die having a first interlayer dielectric layer and a first plurality of electrically conductive structures of first substantially uniform heights with each difference between any two of the first substantially uniform heights being in a range of 1nm to 5nm; and
>
> a second die having a second interlayer dielectric layer and a second plurality of electrically conductive structures of second substantially uniform heights with each difference between any two of the second substantially uniform heights being in a range of 1nm to 5nm, the second die being stacked on the first die, with at least some of the first and second plurality of copper structures being substantially aligned and bonded to each other;

a bus coupled to the semiconductor package; and

a networking interface component coupled to the bus.

Independent claim 19 also includes similar language regarding "substantially uniform heights being in a range of 1nm to 5nm" as indicated in claim 22 above.

Claims 15 and 22 of the instant application also provide language regarding use of the described semiconductor package in conjuction with "a bus coupled to the semiconductor package" and "a networking interface component coupled to the bus." As will be demonstrated below, the claimed configuration is not found in either the '650 reference or the '772 reference.

THE '650 REFERENCE

The '650 reference discloses three-dimensional stacked substrate arrangements with reliable bonding and intersubstrate protection. Pillars in the '650 reference are formed according to a conventional CMP process (see e.g., paragraph **[0024]**). As previously indicated in Applicant's Technical Field and Background, one area of difficulty preventing accomplishment of quality stacking when CMP processes are used to create the copper structures is the non-uniformity of heights of the copper structures relative to the dielectric. This is due to the fact that CMP processes generally result in conventional uniformity of only micrometer scale, which in turn leads to conventional inter-substrate spacing of micrometer scale (see *e.g.*, paragraph **[0028]** of the '650 reference where it is stated that after bonding the inter-substrate spacing is at best "0.01- 0.2 μm"). "0.01- 0.2 μm" translates into a range of 10nm to 200nm or a **variance of over 190nm between heights**. In contrast, the apparatus in claim 1 requires that the copper structures have "substantially uniform heights with each difference ... being 5 nm or less". Claim 15 includes a similar "5nm or less" requirement, and claims 19 and 22 include similar "1nm - 5nm" requirements. Thus, the '650 reference fails to anticipate at least one of the required elements recited in claims 1, 15, 19, and 22.

In the final Office Action, the Examiner asserted that paragraph **[0002]** of the '650 reference anticipates claims 15 and 22 of the instant application. However, paragraph **[0002]** of the '650 reference merely states:

> [0002]Three-dimensional stacked substrate (3D-SS) arrangements are electronic devices having a plurality of stacked semiconductor die/chips/wafers that are physically and electrically interconnected with one another. The drive toward achieving 3D-SSs is in its infancy, and numerous technical problems for achieving 3D-SSs have not yet been satisfactorily resolved. Continued solutions and/or improvements are needed.

While paragraph **[0002]** of the '650 reference provides clear indication of the numerous technical problems yet to be solved in the art, there is no mention, as asserted by the final Office Action in item 3 (c) on page 3, of either "a bus coupled to the semiconductor package" or "a networking interface component coupled to the bus" as recited in claims 15 and 22 of the instant application.

Accordingly, the '650 reference does not anticipate copper structures having "substantially uniform heights with each difference ... being 5 nm or less" as recited in claim 1 and 15 or "in a range of 1nm to 5nm" as recited in claims 19 and 22 of the instant application. Additionally, the '650 reference does not anticipate or even mention, "a networking interface component" as recited in claims 15 and 22 of the instant application.

THE '772 REFERENCE

The '772 reference discloses various methods for bonding wafers using a metal interlayer. The '772 reference indicates that the feature sizes of the conductors are on the order of .1 to 100 μm in paragraph **[0017]** and that conductors 233*u* extend above the upper interconnect layer to heights between 10 and 500 nm in paragraph **[0019]**. In contrast, the apparatus claimed in claim 1 indicates differences "between any two of the ... substantially uniform heights being 5 nm or less" for the first and second "plurality of copper structures". In this manner, the '772 reference fails to anticipate the claimed height uniformity on a nanometer scale as recited in the instant application.

Moreover, the conductor structures 233*u* and 283*u* in the '772 reference are capped with metal interlayers 250 and 290 prior to being interconnected. These metal interlayers 250 and 290 are then bonded together (see e.g., paragraph 0021, Figure 2E, process step 130 of Figure 1, and Figure 2F). In contrast, the second wafer of the apparatus claimed in claim 1 is stacked on the first wafer "with at least some of the first and second plurality of copper structures being substantially aligned and bonded to each other." Thus, the '772 reference also fails to anticipate the required bonding of the copper structures "to each other" as recited in claim 1 of the instant application.

The '772 reference does not anticipate copper structures having "substantially uniform heights with each difference ... being 5 nm or less" as recited in claims 1 and 15 or "in a range of 1nm to 5nm" as recited in claims 19 and 22. Nor does the '772 reference anticipate that "at least some of the first and second plurality of copper structures" are "substantially aligned and bonded to each other" as recited in claims 1, 15, 19, and 22. Furthermore, the '772 reference does not anticipate or even mention "a networking interface component" as recited in claim 15 and claim 22.

Accordingly, it is believed to be clear that none of the references anticipate all the features of claims 1, 15, 19, or 22. Claims 1, 15, 19, and 22 are, therefore, believed to be patentable over the art. The dependent claims 2-3, 16-18, 20-21, and 23-25 are believed to be patentable as well because they all are ultimately dependent on claims 1, 15, 19, or 22.

In the event the Examiner should still find any of the remaining claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested, as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

CONCLUSION

In view of the foregoing, reconsideration and allowance of claims 1-3 and 15-25 is solicited. Accordingly, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present paper, the Examiner is kindly requested to contact the undersigned at (206) 407-1509. If any fees are due in connection with filing this paper, the Commissioner is authorized to charge the Deposit Account of Schwabe, Williamson and Wyatt, P.C., No. 50-0393.

Respectfully submitted,
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